HIGH-K/METAL GATE MOSFET WITH REDUCED PARASITIC CAPACITANCE

FIELD OF THE INVENTION

[0001] The present invention relates to a semiconductor structure and a method of fabricating the same. More particularly, the present invention relates to a metal oxide semiconductor field effect transistor (MOSFET) including a high dielectric constant (k) gate dielectric and a metal-containing gate conductor that has reduced parasitic capacitance. The present invention also provides a method of fabricating such a MOSFET.

BACKGROUND OF THE INVENTION

[0002] In the semiconductor industry, a gate stack including a high-k gate dielectric (a gate dielectric having a dielectric constant of greater than 4.0, typically greater than 7.0) and a metal gate is one of the most promising options for continuing complementary metal oxide semiconductor (CMOS) scaling.

[0003] One of the process schemes for fabricating a high-k/metal gate MOSFET is a replacement gate method. In a replacement gate process, a MOSFET can be fabricated using a sacrificial gate electrode. In such a process, the sacrificial gate electrode is formed first and thereafter the sacrificial gate electrode is replaced by a gate stack including a high-k gate dielectric and a metal gate. Since the gate stack including the high-k gate dielectric and the metal gate is formed after high temperature processing steps such as a source/drain activation anneal, the replacement gate process has the advantage of minimal damage on the high-k gate dielectric and the metal gate. Moreover, a wide range of metals can be selected for the gate conductor.

[0004] One severe drawback of a conventional gate replacement process results in the high-k gate dielectric being present not only beneath the metal gate, but also on vertical sidewalls of the metal gate.

[0005] FIG. **1** is a pictorial representation of a prior art MOSFET including a gate stack comprising a high-k gate dielectric and a metal gate which is fabricated using a conventional gate replacement process as mentioned above. In particular, FIG. **1** shows a prior art MOSFET structure that includes a semiconductor substrate **1000** that has source/drain diffusion regions **1004** located therein. The semiconductor substrate **1000** also contains trench isolation regions **1006** that are filled with a trench dielectric material. Atop the semiconductor substrate **1000**, there is shown a high-k gate dielectric **1008**, which is formed in the shape of a "U", and a metal gate **1010** located within the U-shaped high-k gate dielectric **1008**. A dielectric spacer **1012** is located on outer vertical sidewalls of the U-shaped high-k gate dielectric **1008**. The structure shown in FIG. **1** also includes an interlevel dielectric material **1020** that has contact vias **1022** located therein which extend to the upper surface of the source/drain diffusion regions **1004**. The interlevel dielectric material **1020** is laterally separated from the gate stack by the dielectric spacer **1012**.

[0006] The presence of the metal gate **1010** on the vertical sidewalls of the U-shaped high-k gate dielectric **1008** results in an undesired high contact-to-gate conductor parasitic capacitance.

[0007] Another problem associated with a high-k gate dielectric is that the high-k gate dielectric at the gate corners (represented by the dotted circle shown in FIG. **1**) may not be ideal due to variations in thickness and/or chemical component. A conventional gate reoxidation process cannot be used to strengthen the high-k gate dielectric at the gate corners because the high-k gate dielectric is sealed by the metal gate and the dielectric spacer. The non-ideal high-k gate dielectric at the gate corners results in high leakage and poor reliability.

[0008] In view of the above, there is a need for a new and improved high-k/metal gate MOSFET with reduced contact-to-gate conductor parasitic capacitance and, optionally, an improved high-k gate dielectric at the gate corners.

SUMMARY OF THE INVENTION

[0009] The present invention provides a high-k gate dielectric/metal gate MOSFET that has a reduced contact-to-gate conductor parasitic capacitance as compared to a high-k gate dielectric/metal gate MOSFET fabricated using a conventional gate replacement process. In the present invention, a reduction in the contact-to-gate conductor parasitic capacitance of about 10% or greater is achieved as compared with that of a prior art high-k gate dielectric/metal conductor MOSFET made using a conventional gate replacement process.

[0010] The present invention also provides a high-k gate dielectric/metal gate MOSFET in which an improved high-k gate dielectric is present at the gate corners.

[0011] The present invention further provides, in some embodiments, a high-k gate dielectric/metal gate MOSFET that includes a low-k dielectric spacer located on vertical sidewalls of the metal gate. The low-k dielectric spacer employed has a dielectric constant of less than 4, preferably less than 3.5. The presence of the low-k dielectric spacer aids in further lowering the contact-to-gate conductor parasitic capacitance.

[0012] The present invention even further provides a high-k gate dielectric/metal gate MOSFET in which a channel region located beneath the high-k gate dielectric/metal gate stack has a length of about 2 μm or less.

[0013] In general terms, the present invention provides a semiconductor structure that comprises:

[0014] at least one metal oxide semiconductor field effect transistor (MOSFET) located on a surface of a semiconductor substrate, said at least one MOSFET comprising a gate stack including, from bottom to top, a high-k gate dielectric and a metal-containing gate conductor, said metal-containing gate conductor having gate corners located at a base segment of the metal-containing gate conductor, wherein said metal-containing gate conductor has vertical sidewalls devoid of said high-k gate dielectric except at said gate corners;

[0015] a gate dielectric laterally abutting said high-k gate dielectric present at said gate corners; and

[0016] a gate spacer laterally abutting said metal-containing gate conductor and located upon an upper surface of both the gate dielectric and the high-k gate dielectric that is present at the gate corners.

[0017] The inventive structure further comprises an interlevel dielectric material which contains conductively filled contact vias that extend to the surface of the semiconductor substrate which includes source/drain diffusion regions of the at least one MOSFET.

[0018] In some embodiments of the present invention, the inventive structure may further include a spacer liner present between the gate spacer and the interlevel dielectric material,